**PRACTICAL 3**

**COMPUTER ORGANISATION AND ARCHITECTURE**

|  |  |
| --- | --- |
| **NAME: VARUN KHADAYATE** | **ROLL NO: A016** |
| **PROGRAM: BTECH SY** | **DIVISION: CSBS** |
| **BATCH: 1** | **DATE OF EXPERIMENT: 26/08/2020** |

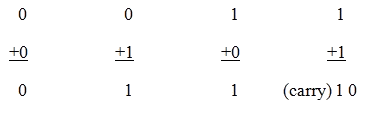
**AIM**

### Construction of half adder using XOR and NAND gates and verification of its operation

**THEORY**

Adders are digital circuits that carry out addition of numbers. Adders are a key component of arithmetic logic unit. Adders can be constructed for most of the numerical representations like Binary Coded Decimal (BDC), Excess – 3, Gray code, Binary etc. out of these, binary addition is the most frequently performed task by most common adders. Apart from addition, adders are also used in certain digital applications like table index calculation, address decoding etc.  
  
Binary addition is similar to that of decimal addition. Some basic binary additions are shown below.

**Schematic representation of half adder**

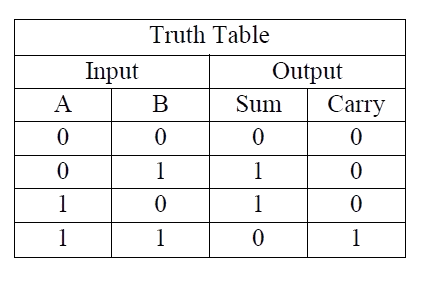
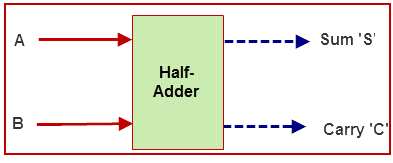


Half adder is a combinational circuit that performs simple addition of two binary numbers. The block diagram of a half adder is shown below.

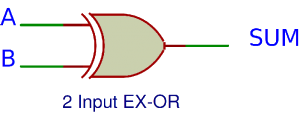
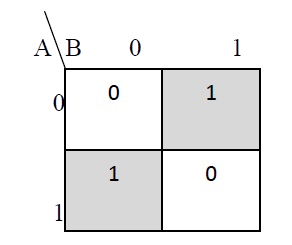
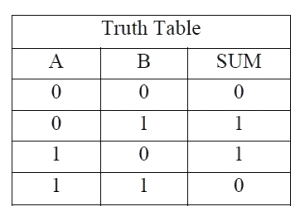
### 1.1) Half Adder Truth Table

If we assume A and B as the two bits whose addition is to be performed, a truth table for half adder with A, B as inputs and Sum, carry as outputs can be tabulated as follows.

The sum output of the binary addition carried out above is similar to that of an Ex-OR operation while the carry output is similar to that of an AND operation. The same can be verified with help of Karnaugh Map.

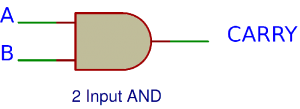
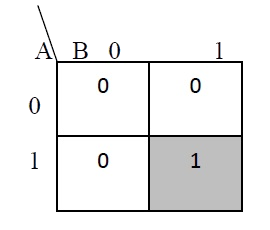
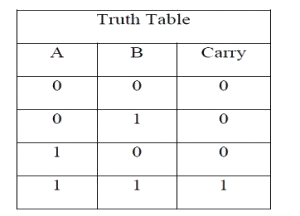


The truth table and K Map simplification for sum output is shown below.



**Sum = A B' + A' B**

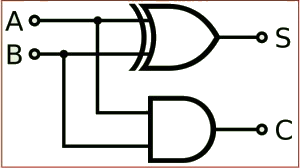
The truth table and K Map simplification for carry is shown below.



**Carry = AB**

If A and B are binary inputs to the half adder, then the logic function to calculate sum S is Ex – OR of A and B and logic function to calculate carry C is AND of A and B. Combining these two, the logical circuit to implement the combinational circuit of half adder is shown below.

**Half Adder Logic Diagram**

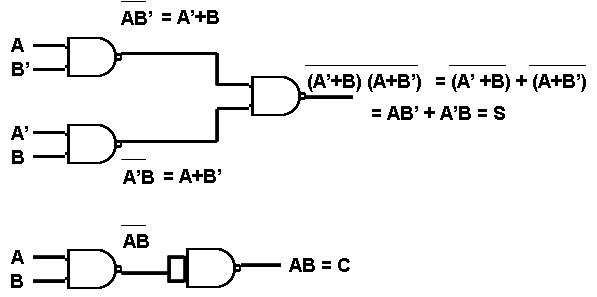


As we know that NAND and NOR are called universal gates as any logic system can be implemented using these two, the half adder circuit can also be implemented using them. We know that a half adder circuit has one Ex – OR gate and one AND gate.

#### 1.2) Half Adder using NAND gates

Five NAND gates are required in order to design a half adder. The circuit to realize half adder using NAND gates is shown below.

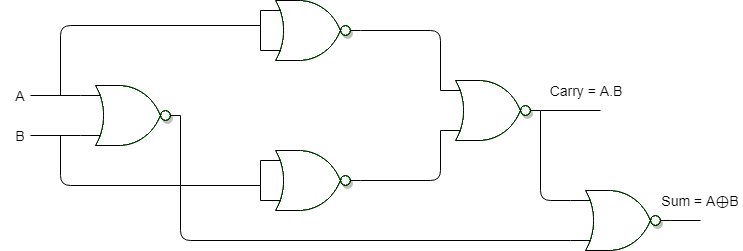
**Realization of half adder using NAND gates**



#### 1.3) Half Adder using NOR gates

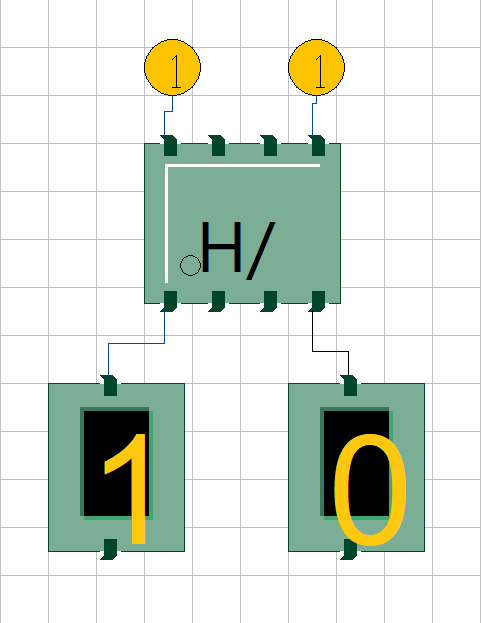
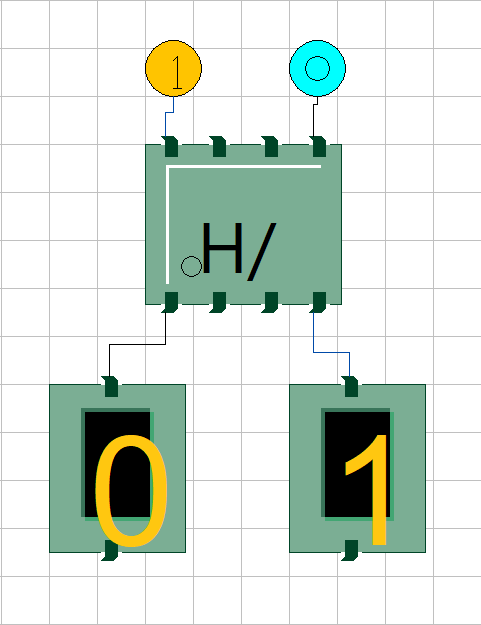
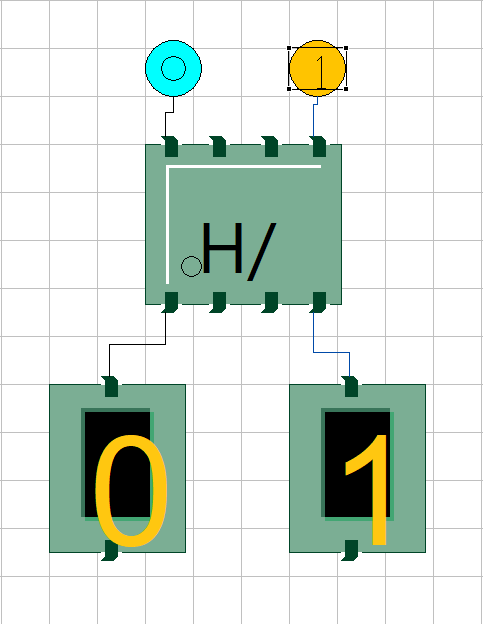
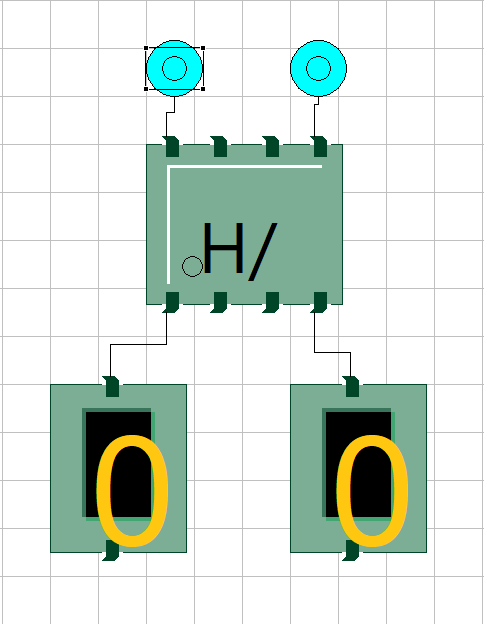
Five NOR gates are required in order to design a half adder. The circuit to realize half adder using NOR gates is shown below.

**Realization of half adder using NOR Gates**

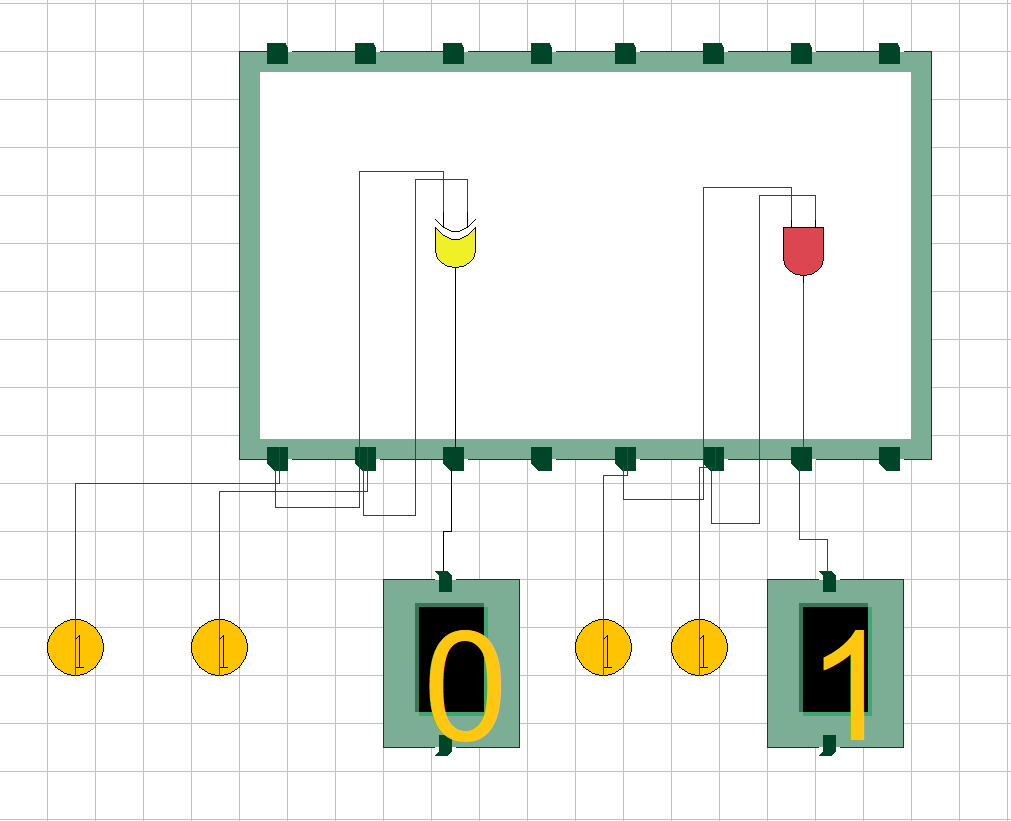
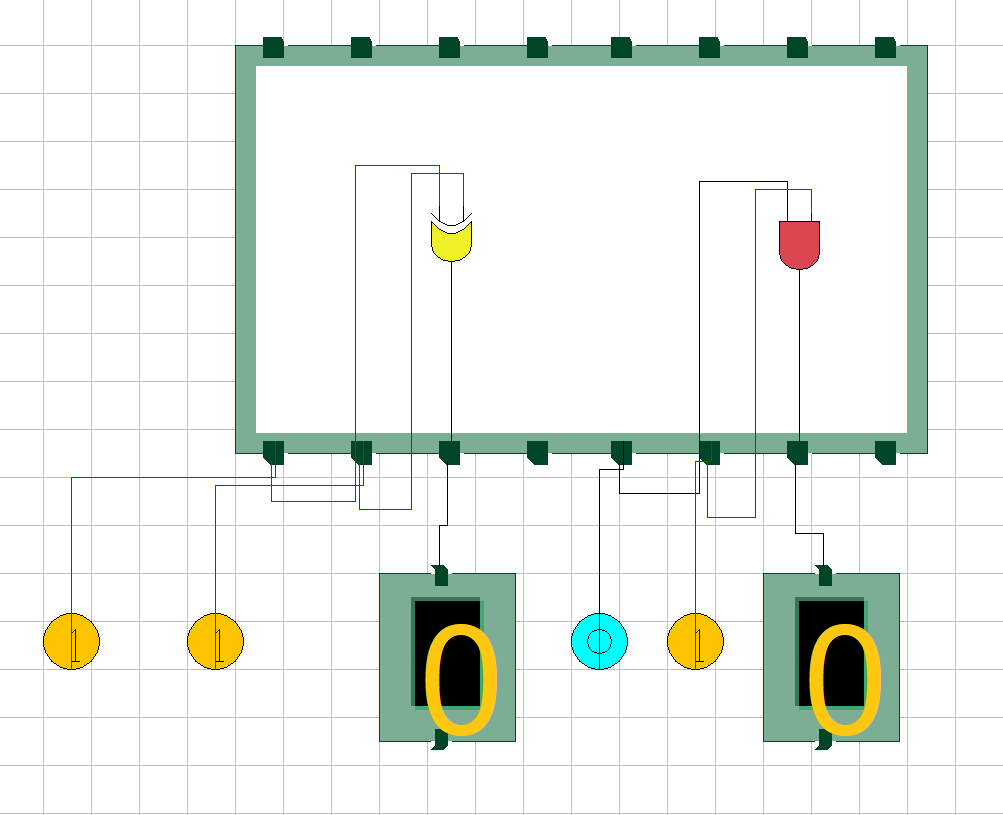
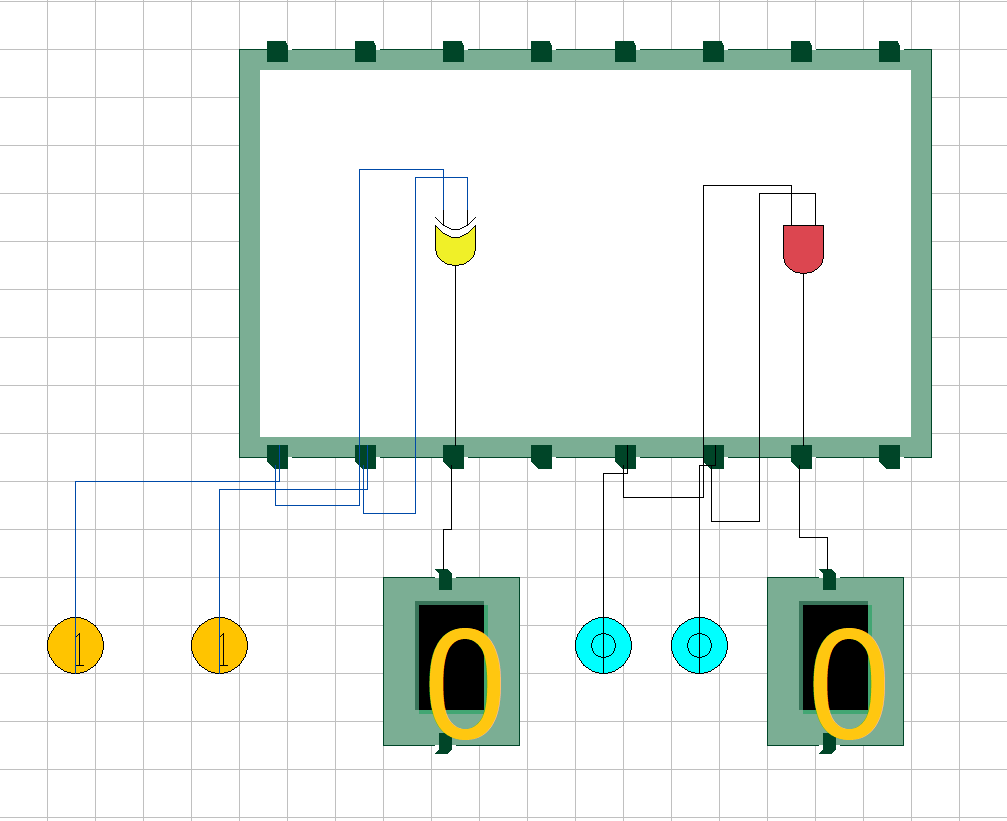
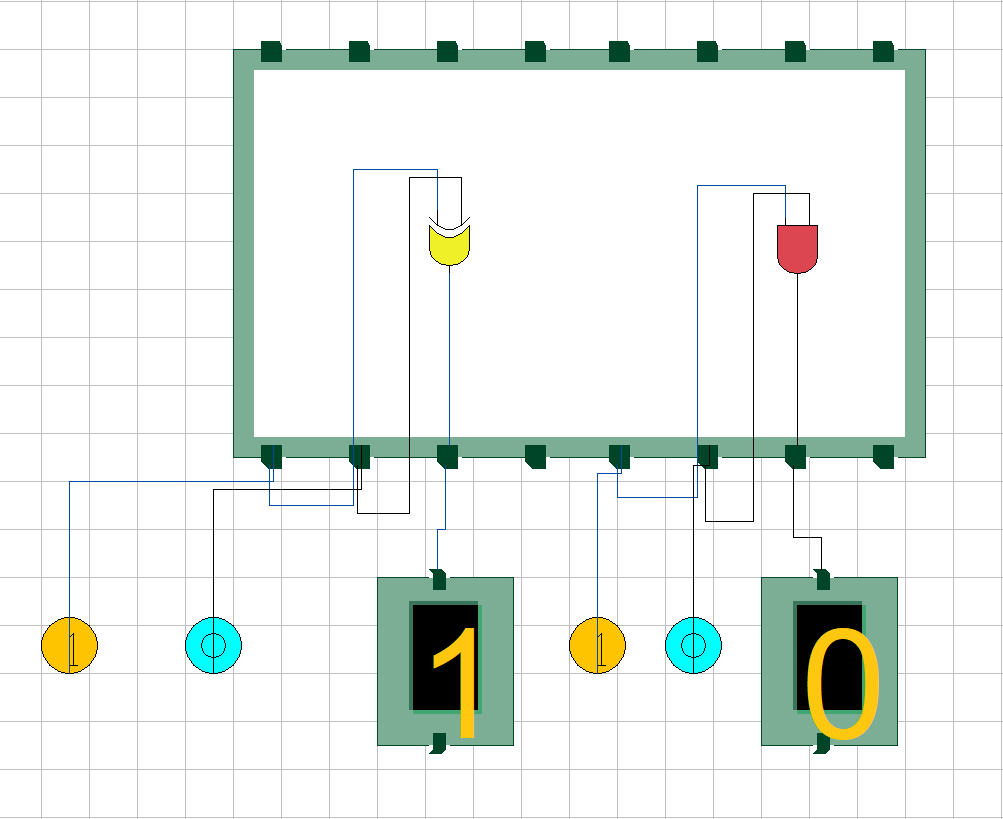
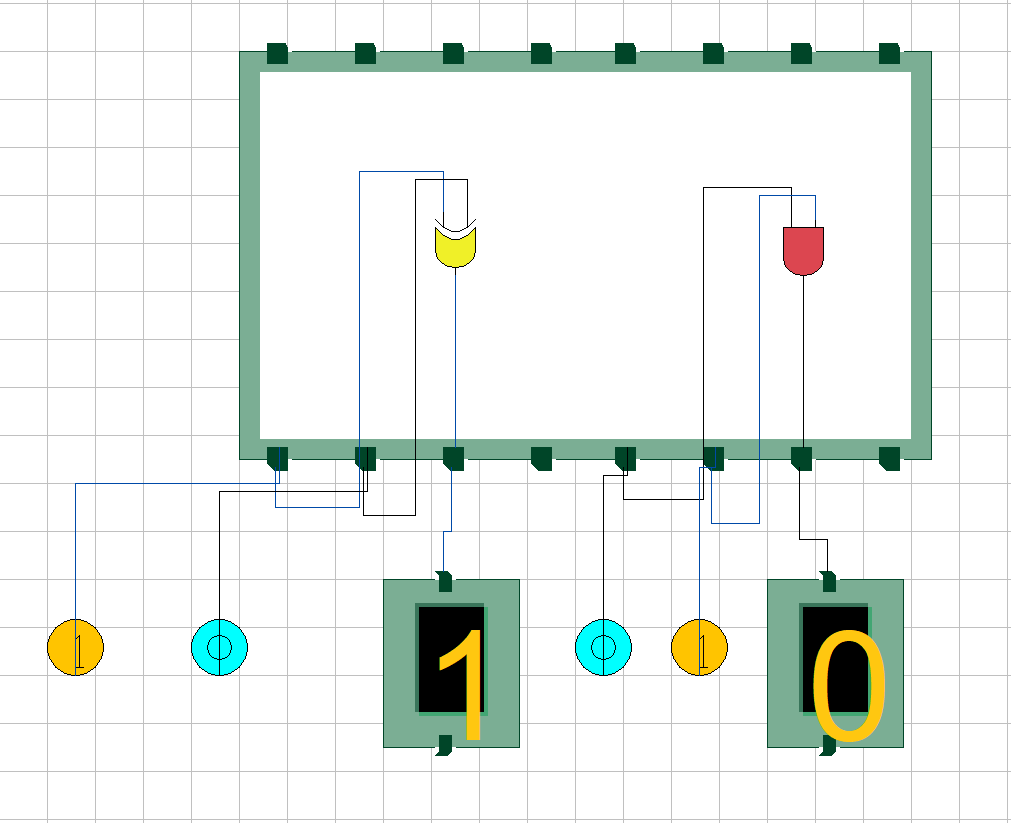
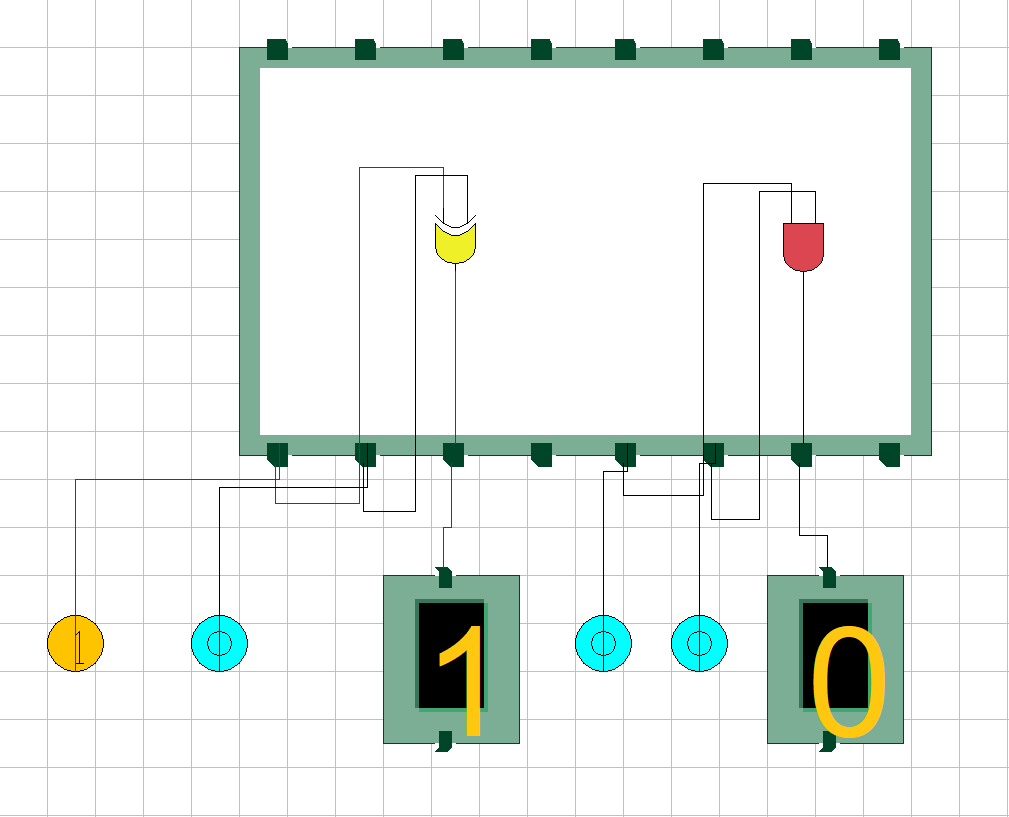
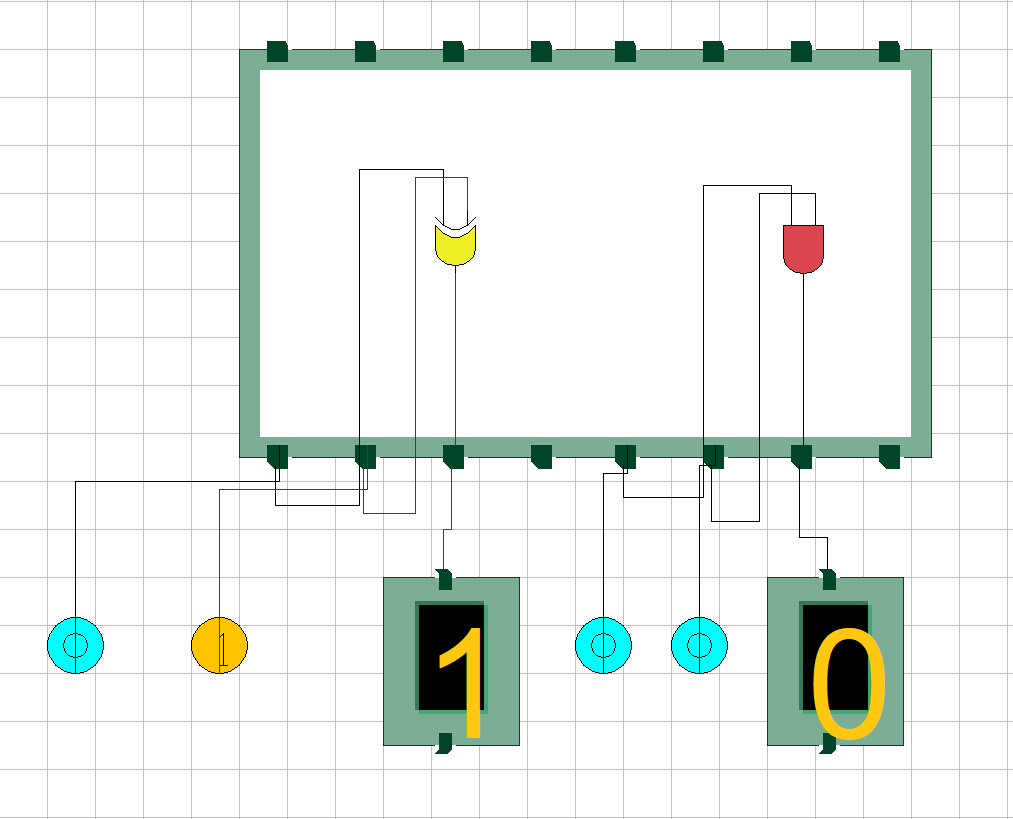
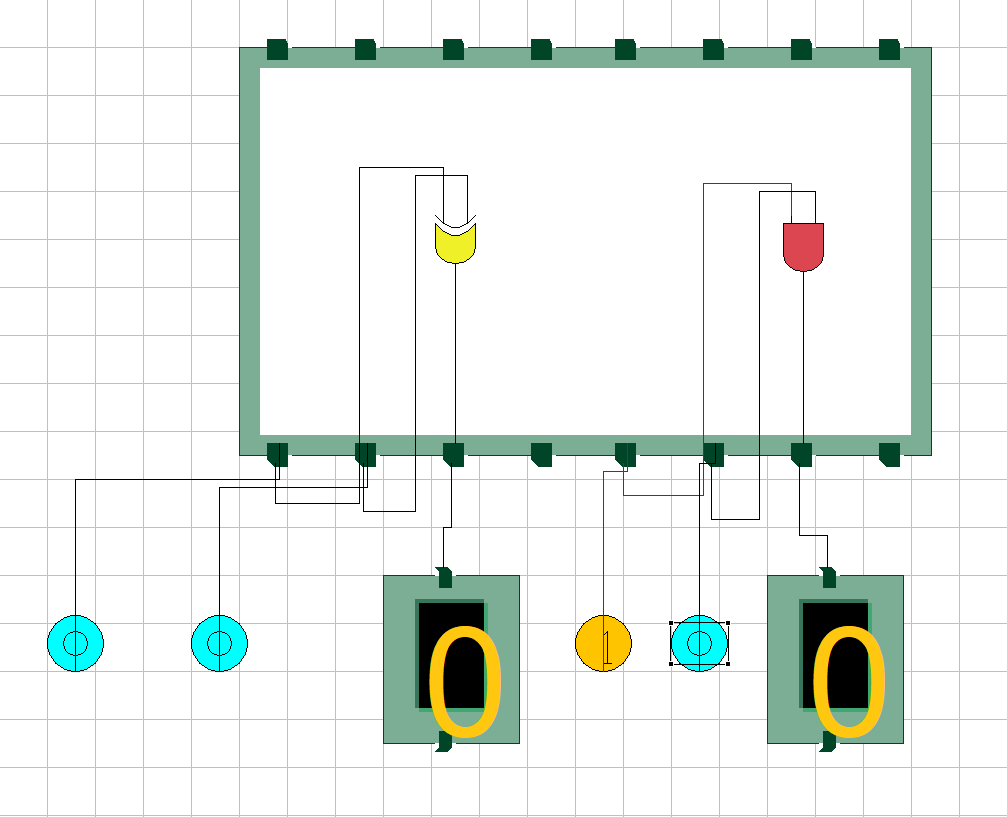
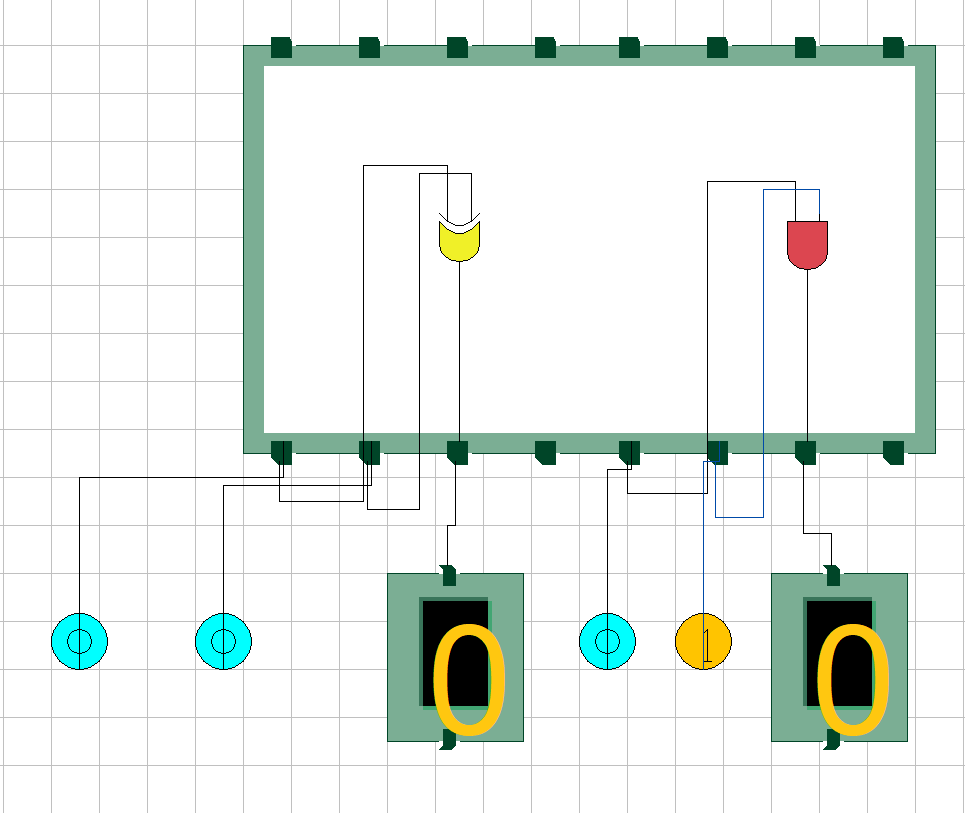
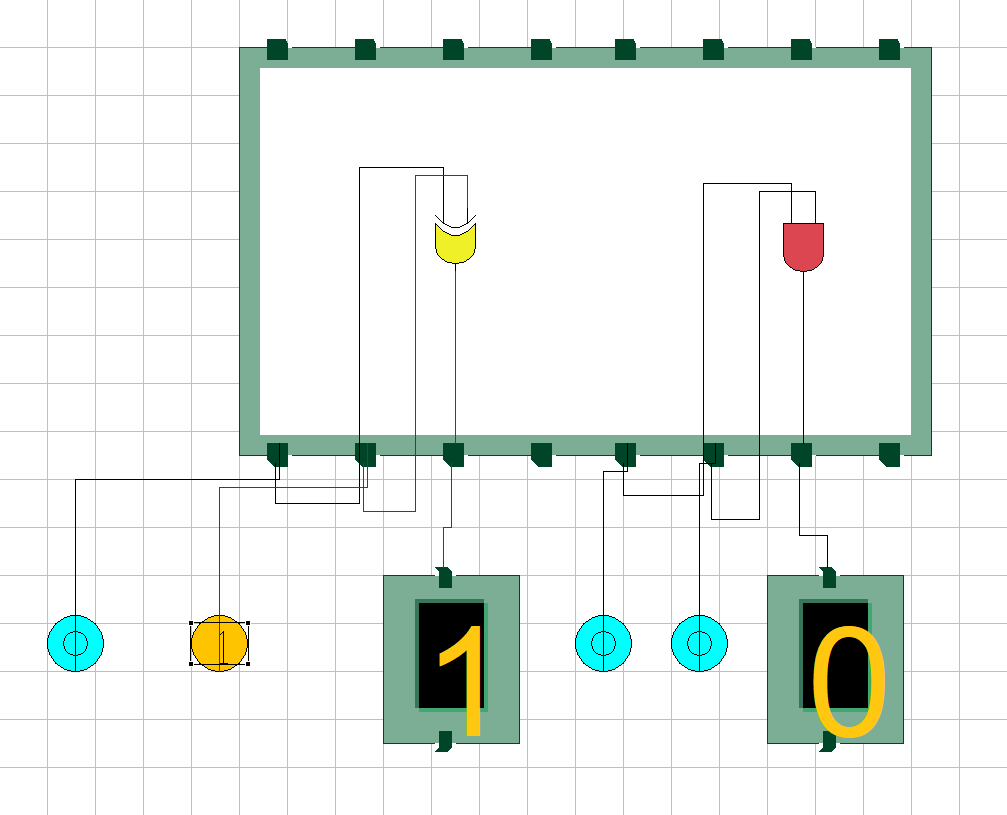
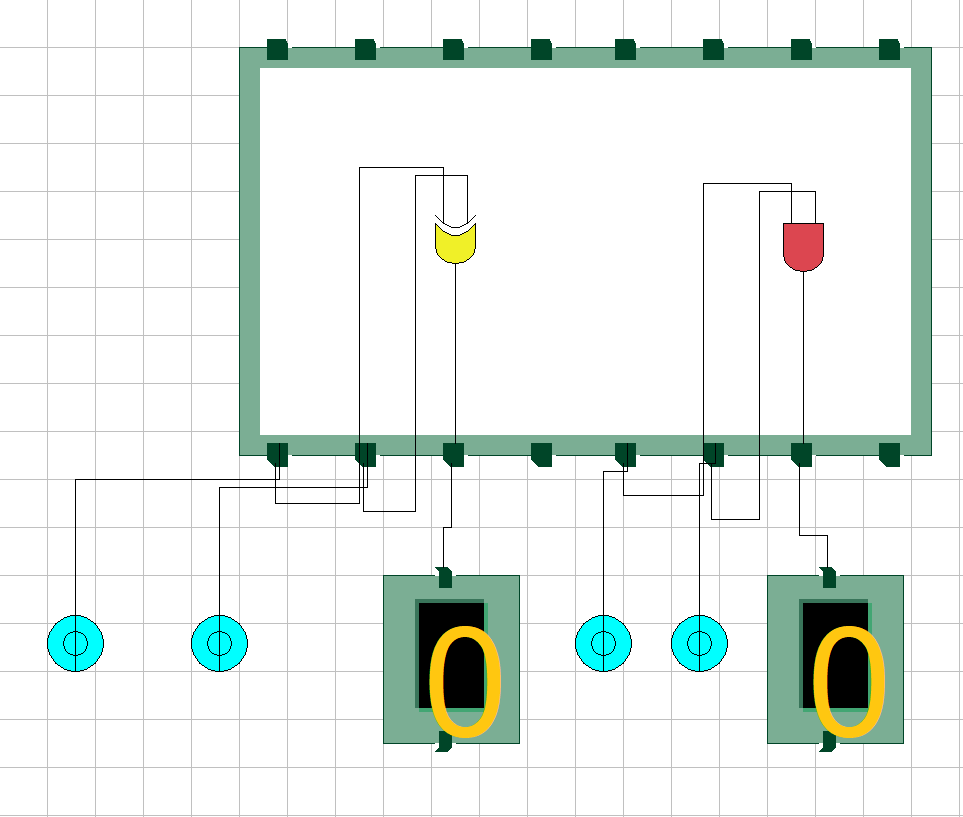


**SIMULATION**

**Dummy Half Adder**



**Half adder using XOR and NAND gates**



**CONCLUSION**

Hence, we are able to verify and study the functionality of a half adder